REMARKS

Claims 1-8, 10-12, 14-20, 23-28, 30 and 32-34 are currently pending in the subject application, and are presently under consideration. Claims 1, 5, 7, 8, 10, 11 and 32 stand rejected. Claims 2-4, 6 and 33 are objected to as being dependent from a rejected base claim, but would be allowable if rewritten in independent form. Favorable reconsideration of the application is requested in view of the amendments and comments herein.

I. Interview Summary

Applicant appreciates the courtesy extended during a telephone interview on December 12, 2005. During the interview, claims 5, 7, 8 were discussed relative to U.S. Patent No. 6,701,445 to Majos and claim 32 was discussed relative to U.S. Patent No. 5,459,435 to Taki. The Examiner indicated that he would reconsider the patentability of these claims 5, 7, 8 and 32 in view of the points raised during the interview; namely, that the cited art was deficient in teaching all the claimed features. This response has been drafted in view of the discussion with the Examiner.

II. Claims 1, 5, 7-8 and 10-11 are patentable over U.S. Patent No. 6,701,445.

Claims 1, 5, 7-8 and 10-11 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,701,445 to Majos ("Majos"). Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claim 1 has been canceled in this response and claims 5 and 7, which depend directly from claim 1, have been rewritten in independent form.

Claim 5 recites a phase detector that compares the phase of the synchronization signal relative to the phase of the clock signal to provide a phase signal, and a phase adjuster that delays the clock signal by an amount based on the phase signal. The Office Action cites column 7, lines 51-55, of Majos to support the contention that claim 5 is anticipated by Majos. The cited section of Majos fails to teach a phase detector and a phase adjuster as recited in claim 5. Instead, the cited section of Majos describes a logic circuit that produces an error signal when the frequency of a data signal Din is at much too high or too low a frequency outside the lock-on band of the VCO (voltage controlled oscillator) or contains non-conform jitter. Majos at Col. 7 lines 48-55. Moreover, the logic circuit being described is implemented as part of the frequency comparator (3), which performs the function shown

in the truth table at Col. 7, lines 30-46. Thus, the section of Majos cited in the Office Action does not teach or suggest the phase detector and phase comparator recited in claim 5.

Majos does disclose a phase comparator (2), which is shown and described in more detail with respect to FIG. 3. The phase comparator (2) taught by Majos, however, does not compare the phase of the synchronization signal relative to the phase of the clock signal to provide a phase signal, as recited in claim 5. Moreover, Majos fails to teach or suggest the use of phase comparator that delays the clock signal based on the phase signal. Instead, Majos teaches that the phase comparator (2) receives the state of the clock signal H produced by the VCO for each transition of the incoming data Din. Majos at Col. 5, lines 14-17. The outputs Q1 and Q3 from the sampling circuit (1) are also provided to the phase comparator (2). Majos at Col. 5, lines 14-17; Col. 5 line 63 through Col. 6, line 2. The phase comparator (2) has logic that is configured to chose "as the clock signal which is more in phase with the data signal Din, either the signal H or its complement $\overline{H}$." Majos at Col. 6, lines 19-22. The selected signal H or its complement $\overline{H}$ is utilized to latch the input data signal Din through the D-type flip flop that is in-phase with the selected clock signal H or $\overline{H}$. Since, the phase comparator (2) of Majos does not compare the phase of the synchronization signal relative to the phase of the clock signal, as recited in claim 5, but instead selects the clock signal H or its complement $\overline{H}$ depending on which is closer to the input data signal Din. Since Majos fails to teach or suggest the recited phase detector and corresponding phase adjuster, as recited in claim 5, Majos does not anticipate claim 5 Reconsideration and allowance of claim 5 and claim 6, which depends from claim 5 and has been indicated as being allowable, are respectfully requested.

Claim 7 has been amended into independent form as well as to recite that the update control sets a variable rate for updating the frequency of the clock signal. Amended claim 7 also recites that the oscillator/control system adjusts the clock signal at an update interval corresponding to the variable rate set by the update control. Support for this amendment can be found, for example, at page 6, line 11, through page 7, line 12, and at page 8, lines 8-25, of the present application.

The Office Action suggests that Majos anticipates claim 7 by contending that delay line (13) generates signal HE that is used to control the frequency of the clock signal H. In contrast to amended claim 7, however, Majos teaches that the sampling system (1) provides the sampling signal HE to a clock input of the upcounter-downcounter (4) that is in phase with the two logic signals H+ and H-. Majos at Col. 5, lines 50-54. From FIG. 2, it is shown

that the sampling signal HE is derived from the data input signal Din by delaying the rising/falling edges of the data signal Din through delay lines (12) and (13). The resulting sampling signal HE is a signal that is in phase with the logic signals H+ and H-, not a variable signal as recited in claim 7. Majos at Col. 5, lines 52-53. Since Majos fails to teach or even suggests that the signal HE might be variable, as recited in amended claim 7, Applicant respectfully submits that claim 7 is patentable. Reconsideration and allowance of amended claim 7 and claims 8, 10 and 11 which depends therefrom are respectfully requested.

Applicant respectfully traverses the rejection of claim 8. The Office Action suggests that claim 8 does not further limit claim 7 and is being treated as an intended use limitation. However, claim 8 adds new features to the system of claim 7. In particular, claim 8 recites that the update control (*e.g.*, circuitry introduced in claim 7) sets the rate for updating the frequency of the clock signal based on an operating characteristic of an IC that comprises the system. Since Majos fails to teach the update control and fails teach the additional functionality of such update control (namely, setting of the variable rate based on an operating characteristic of an IC), claim 8 is patentable over Majos. Accordingly, reconsideration and allowance of claim 8 is respectfully requested.

The Office Action also contends that claims 10 and 11 do not further limit the claim from which they depend. As noted herein, claims 10 and 11 have been amended to depend from claim 7. Accordingly, claims 10 and 11 are allowable for at least the same reasons of claim 7. Additionally, Applicant submits that these claims do further limit claim 7 since such claims recite structural restrictions on the system. For example, claim 10 recites that the system is implemented on an integrated circuit chip, whereas claim 7 contains no such limitation. Similarly, claim 11 recites that the system of claim 7 is implemented on at least n-1 IC chips of an integrated system. Because the Office Action cites no reference that discloses or even suggests the subject matter of claims 10 and 11, Applicant submits that claims 10 and 11 are patentable.

For the reasons stated above, Applicant respectfully requests that the rejection of claims 5, 7-8, and 10-11 be withdrawn.

III. Rejection of Claim 32 Under 35 U.S.C. §103(a)

Claim 32 stands rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,459,435 to Taki (Taki). Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claim 32 has been amended to recite that the system includes an update control controls a variable update interval at which the frequency of the clock signal is updated, the oscillator adjusting the frequency of the internally generated clock signal at the update interval. Support for this amendment can be found, for example, at page 6, line 11, through page 7, line 12, and at page 8, lines 8-25, of the present application. The recited update control of amended claim 7 can be sharply contrasted with any teaching or suggestion provided by Taki.

The Office Action admits that Taki does not disclose an update control that controls the sampling rate which controls a rate at which the frequency of the clock signal is updated and the system is packed in an integrated circuit as called for in the claim. The Office Action states that Taki discloses that the sampling rate of the system is T. The Office Action concludes that the sampling rate T "controls a rate at which the frequency of the clock signal is updated..." Office Action at page 5, lines 11-12. However, as should be evident from amended claim 32, claim 32 does not recite a sampling rate controls a rate at which the frequency of the clock signal is updated, as the Office Action contends. Instead, amended claim 32 recites an update control that controls a variable update interval at which the frequency of the clock signal is updated by the oscillator. The frequency of the output signal f' in Taki might be only indirectly influenced by the chosen sampling rate, for example, such that a faster sampling rate would allow the storage/average unit (3) to average more iterations of the incoming signal f to reduce the effects of noise. However, there is nothing in Taki that would suggest that a different sampling rate T in the system of Taki would change the rate at which the frequency of the clock signal is adjusted by the voltage-controlled X-tal oscillator (7).

Moreover, Taki discloses signals Ta, Tb and Tc, all of which are disclosed as having the same period but different phases as the sampling rate signal T, are used to control and synchronize timing of certain circuit components, namely latches 1b, 2b, 2c and memory 3 and digital to analog converter 6. See Taki at Col. 5, line 48, through Col. 6, line 31 and Figure 2. Significantly, Taki fails to teach or suggest any basis that might lead one skilled in the art to vary the signals Ta, Tb and Tc, or any mechanism for setting an interval at which the frequency of the clock signal is adjusted, as recited in amended claim 32. Thus, Taki and other art of record, taken individually or in combination, fails to teach or suggest the system recited in claim 32.

The Office Action contends that the motivation to modify the sampling rate would be to remove certain noise. As mentioned above, however, there is nothing to suggest that the removal of noise and change in the sampling rate in the system of Taki would vary the interval at which the oscillator adjusts the frequency of the clock signal, as the sampling rate T is disclosed in Taki as being fixed. Applicant submits that if the sampling rate T were set at a rate to remove additional noise and jitter, as suggested in the Office Action, any such sampling rate T would be fixed according to the teachings of Taki. Contrary to the assertion in the Office Action, there is nothing in Taki that would support the proposition that the sampling rate might be variable by an update control nor is there any suggestion or teaching for an oscillator to perform the adjustments to the frequency at an update interval, as recited in claim 32.

For the reasons stated above, Applicant submits that claim 32 is not obvious in view of Taki, individually or in combination with other cited art. Accordingly, applicant respectfully requests reconsideration and allowance of amended claim 32.

IV. Allowable subject matter in Claims 2-4, 6, and 33

Claim 2 has been rewritten in independent form and includes all of the subject matter of canceled claim 1. Claims 3 and 4 depend directly from Claim 2. Claim 6, which has been indicated as containing allowable subject matter, remains dependent on amended claim 5. Claim 33 has been rewritten in independent form and includes all of the subject matter of canceled claim 1. For these reasons, Applicant respectfully requests the objection to claims 2-4, 6, and 33 be withdrawn.

Applicant appreciates the indication that claims 12, 14-20, 23-28, 30, and 34 are allowable.

V. Conclusion

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Should the Examiner have any questions concerning this paper, the Examiner is invited and encouraged to contact Applicant's undersigned attorney at (216) 621-2234, Ext. 106.

An authorization to charge Deposit Account No. 08-2025 for additional fees associated with this amendment on the transmittal sheet submitted with this Response. In the event any additional fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to Deposit Account No. 08-2025.

Respectfully submitted,

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